PATENT

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FOREIGN PATENT DOCUMENTS

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OTHER DOCUMENTS

DF	AD	G. Croft et al., *ESD Protection Techniques for High Frequency Integrated Circuits*, Microelectronics Reliability 38, 1998, pp. 1681-1689.
DF	AE	J. Z. Chen et al., *Design and Layout of a High ESD Performance NPN Structure for Submicron BiCMOS-Bipolar Circuits*, 34th Annual IEEE International Reliability Physics Symposium Proceedings, 1996, pp. 227-232.
DF	AF	J.C. Bernieret al., *A Process Independent ESD Design Methodology*, IEEE International Symposium on Circuits and Systems Proceedings 1, 1999, pp. 218-221.
DF	AG	W.D. Mack et al., *New ESD Protection Schemes for BiCMOS Processes with Application to Cellular Radio Designs*, IEEE International Symposium on Circuits and Systems 6, 1992, pp. 2699-2702.

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